AMENDMENTS TO THE CLAIMS

1. (Currently amended) A decoder for driving a wordline, comprising:

a latch set to a particular state when said wordline is to be driven;

a decoding circuit for receiving and decoding the address of said wordline and setting said latch to said particular state;

a first output inverter, ~~comprising a pair of serially connected complementary CMOS transistors~~ for providing a signal in response to the state of said latch being set to said particular state;

a second output inverter, connected to the output of said first output inverter, and ~~comprising a pair of serially connected complementary CMOS transistors~~ for driving said wordline in response to said latch being set to said particular state; and

a voltage sink, connected to said second output inverter, said voltage sink being at a potential lower than ground.

2-16. (Canceled)

17. (Previously Presented) The decoder of claim 1, further comprising:

a voltage pump for supplying a voltage to said first output inverter.

18. (Canceled)

19. (Currently amended) An method of operating a wordline decoder, comprising:

decoding wordline address information and setting a latch associated with a wordline to a predetermined state when an address of said wordline is decoded;

driving a signal line with [[an]] a first output inverter having an input connected to an output of said latch; ~~and~~

driving said selected wordline with a second output inverter having an input connected to an output of said first output inverter; and

driving said selected wordline with said second output inverter to a voltage below ground when turning off said wordline.

20. (Currently amended) The method of claim 19, further comprising:

supplying a voltage from a voltage pump to said first output inverter for turn on said wordline.

21. (Currently amended) The method of claim 19, further comprising:

supplying a voltage sink to said second output inverter for turning off said wordline.

22. (Canceled)

23. (Currently amended) The method of fabricating a decoder, comprising:

fabricating a latch configured to be set to a particular state when ~~said~~ a wordline is to be driven;

fabricating a decoding circuit for receiving and decoding the address of said wordline and setting said latch to said particular state;

fabricating a first output inverter, comprising a pair of serially connected complementary CMOS transistors for providing a signal in response to the state of said latch being set to said particular state, ~~and~~

fabricating a second output inverter, connected to the output of said first output inverter, and comprising a pair of serially connected complementary CMOS transistors for driving said wordline in response to said latch being set to said particular state; and

fabricating a voltage sink being connected to said second output inverter, said voltage sink for operating at a potential lower than ground.

24. (Previously Presented) The method according to claim 23, further comprising fabricating a voltage pump for supplying a voltage to said first output inverter.

25. (Canceled)